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1 Packet classification using tuple space search 85%
V. Srinivasan , S. Suri , G. Varghese
ACM SIGCOMM Computer Communication Review , Proceedings of the conference on Applications, technologies, architectures, and protocols for computer communication August 1999
Volume 29 Issue 4
Routers must perform packet classification at high speeds to efficiently implement functions such as firewalls and QoS routing. Packet classification requires matching each packet against a database of filters (or rules), and forwarding the packet according to the highest priority filter. Existing filter schemes with fast lookup time do not scale to large filter databases. Other more scalable schemes work for 2-dimensional filters, but their lookup times degrade quickly with each additional dime ...

2 IP switching—ATM under IP 84%
Peter Newman , Greg Minshall , Thomas L. Lyon
IEEE/ACM Transactions on Networking (TON) April 1998
Volume 6 Issue 2

3 Sirpent: a high-performance internetworking approach 82%
D. R. Cheriton
ACM SIGCOMM Computer Communication Review , Symposium proceedings on Communications architectures & protocols August 1989
Volume 19 Issue 4
A clear target for computer communication technology is to support a high-performance global internetwork. Current internetworking approaches use either concatenated virtual circuits, as in X.75, or a "universal" internetwork datagram, as in the DoD Internet IP protocol and the ISO connectionless network protocol (CLNP).

10/041,028

Both approaches have significant disadvantages. This paper describes Sirpent™ (Source Internetwork Routing Protocol with Extended Network Trans ...

4 The click modular router 82%

Eddie Kohler , Robert Morris , Benjie Chen , John Jannotti , M. Frans Kaashoek
ACM Transactions on Computer Systems (TOCS) August 2000
Volume 18 Issue 3

Clicks is a new software architecture for building flexible and configurable routers. A Click router is assembled from packet processing modules called elements. Individual elements implement simple router functions like packet classification, queuing, scheduling, and interfacing with network devices. A router configurable is a directed graph with elements at the vertices; packets flow along the edges of the graph. Several features make individual elements more powerful and ...

5 A unified header compression framework for low-bandwidth links 82%

Jeremy Lilley , Jason Yang , Hari Balakrishnan , Srinivasan Seshan
Proceedings of the 6th annual international conference on Mobile computing and networking August 2000

Compressing protocol headers has traditionally been an attractive way of conserving bandwidth over low-speed links, including those in wireless systems. However, despite the growth in recent years in the number of end-to-end protocols beyond TCP/IP, header compression deployment for those protocols has not kept pace. This is in large part due to complexities in implementation, which often requires a detailed knowledge of kernel internals, and a lack of a common way of pursuing the general p ...

6 Building a robust software-based router using network processors 82%

Tammo Spalink , Scott Karlin , Larry Peterson , Yitzchak Gottlieb
ACM SIGOPS Operating Systems Review , Proceedings of the eighteenth ACM symposium on Operating systems principles October 2001
Volume 35 Issue 5

Recent efforts to add new services to the Internet have increased interest in software-based routers that are easy to extend and evolve. This paper describes our experiences using emerging network processors---in particular, the Intel IXP1200---to implement a router. We show it is possible to combine an IXP1200 development board and a PC to build an inexpensive router that forwards minimum-sized packets at a rate of 3.47Mpps. This is nearly an order of magnitude faster than existing pure PC-base ...

7 Network support for mobile multimedia using a self-adaptive distributed proxy 80%

Zhuoqing Morley Mao , Hoi-sheung Wilson So , Byunghoon Kang
Proceedings of the 11th international workshop on Network and operating systems support for digital audio and video January 2001

Recent advancements in video and audio codec technologies~(e.g., RealV ideo [18] make multimedia streaming possible across a wide range of network conditions. With an increasing trend of ubiquitous connectivity, more and more areas have overlapping coverage of multiple wired and wireless networks. Because the best network service changes as the user moves, to provide good multimedia application performance, the service needs to adapt to user movement as well as network and computational res ...

8 Router plugins: a software architecture for next-generation routers 80%

Dan Decasper , Zubin Dittia , Guru Parulkar , Bernhard Plattner
IEEE/ACM Transactions on Networking (TON) February 2000

Volume 8 Issue 1

9 BPF+: exploiting global data-flow optimization in a generalized packet filter architecture 80%

Andrew Begel , Steven McCanne , Susan L. Graham

ACM SIGCOMM Computer Communication Review , Proceedings of the conference on Applications, technologies, architectures, and protocols for computer communication August 1999

Volume 29 Issue 4

A *packet filter* is a programmable selection criterion for classifying or selecting packets from a packet stream in a generic, reusable fashion. Previous work on packet filters falls roughly into two categories, namely those efforts that investigate flexible and extensible filter abstractions but sacrifice performance, and those that focus on low-level, optimized filtering representations but sacrifice flexibility. Applications like network monitoring and intrusion detection, however, requ ...

10 aItPm: a strategy for integrating IP with ATM 80%

Guru Parulkar , Douglas C. Schmidt , Jonathan S. Turner

ACM SIGCOMM Computer Communication Review , Proceedings of the conference on Applications, technologies, architectures, and protocols for computer communication October 1995

Volume 25 Issue 4

This paper describes research on new methods and architectures that enable the synergistic combination of IP and ATM technologies. We have designed a highly scalable gigabit IP router based on an ATM core and a set of tightly coupled general-purpose processors. This a^{I}t^{P}m (pronounced "IP on ATM" or, if you prefer, "ip-attem") architecture provides flexibility in congestion control, routing, resource management, and packe ...

11 Anatomy of a message in the Alewife multiprocessor 80%

John Kubiatowicz , Anant Agarwal

Proceedings of the 7th international conference on Supercomputing August 1993

Shared-memory provides a uniform and attractive mechanism for communication. For efficiency, it is often implemented with a layer of interpretive hardware on top of a message-passing communications network. This interpretive layer is responsible for data location, data movement, and cache coherence. It uses patterns of communication that benefit common programming styles, but which are only heuristics. This suggests that certain styles of communication may benefit from direct access to the ...

12 Distributed systems - programming and management: On remote procedure call 80%

Patrícia Gomes Soares

Proceedings of the 1992 conference of the Centre for Advanced Studies on Collaborative research - Volume 2 November 1992

The Remote Procedure Call (RPC) paradigm is reviewed. The concept is described, along with the backbone structure of the mechanisms that support it. An overview of works in supporting these mechanisms is discussed. Extensions to the paradigm that have been proposed to enlarge its suitability, are studied. The main contributions of this paper are a standard view and classification of RPC mechanisms according to different perspectives, and a snapshot of the paradigm in use today and of goals for t ...

13 Implementing multidestination worms in switch-based parallel systems: architectural alternatives and their impact 80%

Craig B. Stunkel , Rajeev Sivaram , Dhabaleswar K. Panda
ACM SIGARCH Computer Architecture News , Proceedings of the 24th annual international symposium on Computer architecture May 1997
Volume 25 Issue 2

Multidestination message passing has been proposed as an attractive mechanism for efficiently implementing multicast and other collective operations on direct networks. However, applying this mechanism to switch-based parallel systems is non-trivial. In this paper we propose alternative switch architectures with differing buffer organizations to implement multidestination worms on switch-based parallel systems. First, we discuss issues related to such implementation (deadlock-freedom, replicatio ...

14 BANANAS: an evolutionary framework for explicit and multipath routing in the internet 77%

H. Tahilramani Kaur , S. Kalyanaraman , A. Weiss , S. Kanwar , A. Gandhi
ACM SIGCOMM Computer Communication Review , Proceedings of the ACM SIGCOMM workshop on Future directions in network architecture August 2003
Volume 33 Issue 4

Today the Internet offers a single path between end-systems even though it intrinsically has a large multiplicity of paths. This paper proposes an evolutionary architectural framework "BANANAS" aimed at simplifying the introduction of multipath routing in the Internet. The framework starts with the observation that a path can be encoded as a short hash ("PathID") of a sequence of globally known identifiers. The PathID therefore has global significance (unlike MPLS or ATM labels). This property a ...

15 Hash-based IP traceback 77%

Alex C. Snoeren
ACM SIGCOMM Computer Communication Review , Proceedings of the 2001 conference on Applications, technologies, architectures, and protocols for computer communications August 2001
Volume 31 Issue 4

16 A simple method for extracting models for protocol code 77%

David Lie , Andy Chou , Dawson Engler , David L. Dill
ACM SIGARCH Computer Architecture News , Proceedings of the 28th annual international symposium on Computer architecture May 2001
Volume 29 Issue 2

The use of model checking for validation requires that models of the underlying system be created. Creating such models is both difficult and error prone and as a result, verification is rarely used despite its advantages. In this paper, we present a method for automatically extracting models from low level software implementations. Our method is based on the use of an extensible compiler system, xg++, to perform the extraction. The extracted model is combined with a model of the ha ...

17 LimitLESS directories: A scalable cache coherence scheme 77%

David Chaiken , John Kubiatowicz , Anant Agarwal
Proceedings of the fourth international conference on Architectural support for programming languages and operating systems April 1991
Volume 26 , 19 , 25 Issue 4 , 2 , Special Issue

18 Transport protocol processing at GBPS rates 77%

N. Jain , M. Schawrtz , T. Bashkow

ACM SIGCOMM Computer Communication Review , Proceedings of the ACM symposium on Communications architectures & protocols August 1990

Volume 20 Issue 4

This paper proposes an architecture for accomplishing transport protocol processing at Gbps rates. The limitations of currently used transport protocols have been analyzed extensively in recent literature. Several benchmark studies have established the achievable throughput of ISO TP4 and TCP to be in the low Mbps range; several new protocols and implementation techniques have been proposed to achieve 100 Mbps and higher throughput rates. We briefly review some of these protocols and establ ...

19 Stateful distributed interposition 77%

John Reumann , Kang G. Shin

ACM Transactions on Computer Systems (TOCS) February 2004

Volume 22 Issue 1

Interposition-based system enhancements for multitiered servers are difficult to build because important system context is typically lost at application and machine boundaries. For example, resource quotas and user identities do not propagate easily between cooperating services that execute on different hosts or that communicate with each other via intermediary services. Application-transparent system enhancement is difficult to achieve when such context information is obscured by complex servic ...

20 Design and Implementation of High-Performance Memory Systems for Future Packet Buffers 77%

Jorge García , Jesús Corbal , Llorenç Cerdà , Mateo Valero

Proceedings of the 36th Annual IEEE/ACM International Symposium on Microarchitecture December 2003

In this paper we address the design of a future high-speedrouter that supports line rates as high as OC-3072 (160 Gb/s),around one hundred ports and several service classes. Buildingsuch a high-speed router would raise many technological problems,one of them being the packet buffer design, mainly becausein router design it is important to provide worst-case bandwidthguarantees and not just average-case optimizations.A previous packet buffer design provides worst-case bandwidthguarantees by using ...

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